Amendments to the Claims

This listing of the Claims will replace all prior versions and listings of the claims in this patent application.

Listing of the Claims

1-7. (canceled)

8. (currently amended) A method for fabricating a CMOS semiconductor device structure comprising:

providing a dielectric layer on a substrate;

depositing a hafnium nitride layer overlying said dielectric layer;

depositing a capping layer overlying said hafnium nitride layer;

patterning said hafnium nitride layer and said capping layer and said dielectric layer to form ~~a~~ CMOS gate electrodes; and

forming source and drain regions within said substrate adjacent to said CMOS gate electrodes.

9. (original) The method according to Claim 8 wherein said depositing of said hafnium nitride layer comprises flowing Nitrogen and Argon atoms into a chamber simultaneously wherein said chamber contains said substrate and a hafnium target.

10 . (original) The method according to claim 9 wherein argon and nitrogen flow rates are kept as constant at 25 sccm and 5 sccm, respectively.

11. (currently amended) The method according to Claim 8 wherein said dielectric layer comprises $HfO\cancel{2}_2$ and is deposited at 400°C using a MOCVD cluster tool.

12. (currently amended) The method according to Claim 8 wherein said dielectric layer comprises $HfO\cancel{2}_2$ and wherein said dielectric layer is subjected to post-deposition annealing (PDA) at 700°C in a $N\cancel{2}_2$ ambient.

13. (currently amended) The method according to Claim 8 further comprising adjusting the Nitrogen and Hafnium atomic ratio of said hafnium nitride layer to adjust the work-function of said gate electrodes wherein said atomic ratio of nitrogen to hafnium remains greater than or equal to one.

14. (currently amended) The method according to Claim 8 further comprising impurity doping into said hafnium nitride layer to tune the work-function of said gate electrodes.

15. (original) The method according to Claim 8 further comprising thermal treatment of said hafnium nitride layer by RTA at about 1000 °C for about 20 seconds.

16. (currently amended) A method for fabricating a CMOS semiconductor device structure comprising:

providing a dielectric layer on a substrate;

depositing a first metal layer overlying said dielectric layer;

patterning said first metal layer and said dielectric layer to form ~~a~~CMOS gate electrodes; and

forming source and drain regions within said substrate adjacent to said CMOS gate electrodes.

17. (original) The method according to Claim 16 wherein said depositing of said first metal layer comprises flowing Nitrogen and Argon atoms into a chamber simultaneously wherein said chamber contains said substrate and a hafnium target to form a hafnium nitride first metal layer.

18 . (original) The method according to claim 17 wherein argon and nitrogen flow rates are kept as constant at 25 sccm and 5 sccm, respectively.

19. (currently amended) The method according to Claim 16 wherein said dielectric layer comprises $HfO\sout{2}_2$ and is deposited at 400°C using a MOCVD cluster tool.

20. (currently amended) The method according to Claim 16 wherein said dielectric layer comprises $HfO\sout{2}_2$ and wherein said dielectric layer is subjected to post-deposition annealing (PDA) at 700°C in a $N\sout{2}_2$ ambient.

21. (currently amended) The method according to Claim 17 further comprising adjusting the Nitrogen ~~and Hafnium atomic ratio of said hafnium nitride layer~~ flow rate to adjust the work-function of said gate electrodes wherein said atomic ratio of nitrogen to hafnium remains greater than or equal to one.

22. (currently amended) The method according to Claim 17 further comprising impurity doping into said hafnium nitride layer to tune the work-function of said gate electrodes.

23. (original) The method according to Claim 17 further comprising thermal treatment of said hafnium nitride layer by RTA at about 1000 °C for about 20 seconds.

24. (original) The method according to Claim 17 further comprising:

depositing a second metal capping layer overlying said first metal layer prior to said patterning wherein said second metal is different from said first metal.

25. (original) The method according to Claim 24 wherein said first metal layer comprises tungsten or tantalum nitride and wherein said second metal layer comprises hafnium nitride.

26. (original) The method according to Claim 24 wherein said first metal layer comprises hafnium nitride and wherein said second metal layer comprises tungsten or tantalum nitride.

27. (original) The method according to Claim 24 wherein said first and second metal layers are deposited by physical vapor deposition or chemical vapor deposition.

28-34. (canceled)

35. (new) A method for fabricating a CMOS semiconductor device structure comprising:

providing a dielectric layer on a substrate;

depositing a hafnium nitride layer overlying said dielectric layer;

depositing a titanium nitride or tungsten capping layer overlying said hafnium nitride layer;

patterning said hafnium nitride layer and said capping layer and said dielectric layer to form CMOS gate electrodes; and

forming source and drain regions within said substrate adjacent to said CMOS gate electrodes.

36. (new) The method according to Claim 35 wherein said depositing of said hafnium nitride layer comprises flowing Nitrogen and Argon atoms into a chamber simultaneously wherein said chamber contains said substrate and a hafnium target.

37. (new) The method according to Claim 35 wherein said dielectric layer comprises HfO_2.

38. (new) The method according to Claim 36 further comprising adjusting the Nitrogen flow rate to adjust the work-function of said gate electrodes wherein the atomic ratio of nitrogen to hafnium in said hafnium nitride layer remains greater than or equal to one.

39. (new) The method according to Claim 35 further comprising impurity doping into said hafnium nitride layer to tune the work-function of said gate electrodes.

40. (new) A method for fabricating a CMOS semiconductor device structure comprising:

providing a dielectric layer on a substrate;

depositing a first metal layer overlying said dielectric layer;

depositing a second metal capping layer overlying said first metal layer;

patterning said first metal layer, said second metal capping layer, and said dielectric layer to form CMOS gate electrodes; and

forming source and drain regions within said substrate adjacent to said CMOS gate electrodes.

41. (new) The method according to Claim 40 wherein said dielectric layer comprises HfO_2.

42. (new) The method according to Claim 40 wherein said first and second metal layers are deposited by physical vapor deposition or chemical vapor deposition.

43. (new) The method according to Claim 40 wherein said first metal layer comprises tungsten or tantalum nitride and wherein said second metal layer comprises hafnium nitride.

44. (new) The method according to Claim 43 wherein said depositing of said second metal layer comprises flowing Nitrogen and Argon atoms into a chamber simultaneously wherein said

chamber contains said substrate and a hafnium target to form said hafnium nitride second metal layer.

45. (new) The method according to Claim 44 further comprising adjusting the flow rate to adjust the work-function of said gate electrodes wherein the atomic ratio of nitrogen to hafnium remains greater than or equal to one.

46. (new) The method according to Claim 44 further comprising impurity doping into said hafnium nitride layer to tune the work-function of said gate electrodes.

47. (new) The method according to Claim 44 further comprising thermal treatment of said hafnium nitride layer by RTA at about 1000 °C for about 20 seconds.

48. (new) The method according to Claim 40 wherein said first metal layer comprises hafnium nitride and wherein said second metal layer comprises tungsten or tantalum nitride.

49. (new) The method according to Claim 48 wherein said depositing of said first metal layer comprises flowing Nitrogen and Argon atoms into a chamber simultaneously wherein said chamber contains said substrate and a hafnium target to form said hafnium nitride first metal layer.

50. (new) The method according to Claim 49 further comprising adjusting the flow rate to adjust the work-function of said gate electrodes wherein the atomic ratio of nitrogen to hafnium remains greater than or equal to one.

51. (new) The method according to Claim 49 further comprising impurity doping into said hafnium nitride layer to tune the work-function of said gate electrodes.

52. (new) The method according to Claim 49 further comprising thermal treatment of said hafnium nitride layer by RTA at about 1000 °C for about 20 seconds.